

### (5 pts) Exercise 7-1: Direct Mapped Cache

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Memory	Cache (N = 5)	Processor												
20	<table border="1"> <thead> <tr> <th>Address</th> <th>Data</th> </tr> </thead> <tbody> <tr><td>0</td><td></td></tr> <tr><td>1</td><td></td></tr> <tr><td>2</td><td></td></tr> <tr><td>3</td><td></td></tr> <tr><td>4</td><td></td></tr> </tbody> </table>	Address	Data	0		1		2		3		4		1. Read 30
Address		Data												
0														
1														
2														
3														
4														
21		2. Read 31												
22		3. Read 30												
23		4. Read 26												
24		5. Read 25												
25		6. Read 28												
26	7. Read 23													
27	8. Read 25													
28	9. Read 28													
29														
30														
31														

Total hits?  
Total misses?

### (5 pts) Exercise 7-2: Direct Mapped Cache

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Memory	Cache (N = 4)	Processor										
20	<table border="1"> <thead> <tr> <th>Address</th> <th>Data</th> </tr> </thead> <tbody> <tr><td>0</td><td></td></tr> <tr><td>1</td><td></td></tr> <tr><td>2</td><td></td></tr> <tr><td>3</td><td></td></tr> </tbody> </table>	Address	Data	0		1		2		3		1. Read 30
Address		Data										
0												
1												
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3												
21		2. Read 31										
22		3. Read 30										
23		4. Read 26										
24		5. Read 25										
25		6. Read 28										
26		7. Read 23										
27	8. Read 25											
28	9. Read 28											
29												
30												
31												

Total hits?  
Total misses?

## (5 pts) Exercise 7-6

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- Look back at Exercises 1 and 2 and identify at least two different kinds of reasons for why there might be a cache miss.
  
- How might you possibly address each type of miss?

## (5 pts) Exercise 7-11 – Show final cache and total hits

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Block size = 2, N = 4

Memory		Cache			Processor
Address	Data	Address	Data		
20	7	0			1. Read 16
21	3				2. Read 14
22	27				3. Read 17
23	32				4. Read 13
24	101	1			5. Read 24
25	78				6. Read 17
26	59	2			7. Read 15
27	24				8. Read 25
28	56	3			9. Read 27
29	87				
30	36				
31	98				

Total # hits?

## (5 pts) Exercise 7-12

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- Show the correct formula for calculating the cache index, given the cache parameters below

1. N = 10, Block size = 4
  
2. N = 8, Block size = 1, Associativity = 4
  
3. N = 16, Block size = 8, Associativity = 2

## (5 pts) Exercise 7-13 – Fill in blanks, show final cache & total hits

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Block size = \_\_\_\_\_, N = \_\_\_\_\_, Assoc = \_\_\_\_\_

Memory

20	7
21	3
22	27
23	32
24	101
25	78
26	59
27	24
28	56
29	87
30	36
31	98

Cache

		Address	Data	
0				
1				

Processor

1. Read 24
2. Read 25
3. Read 26
4. Read 24
5. Read 21
6. Read 26
7. Read 24
8. Read 26
9. Read 27

## (15 pts) Exercise 7-16

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- Assume you have an empty cache with a total of 16 blocks, with each block having 2 bytes. In this exercise, the cache is direct mapped.
- At right is a series of byte addresses. You should:
  1. Label each one as a hit or miss
  2. Draw the cache and show the final contents of the cache

As always, show your work.

Address	Hit / Miss?
2	
3	
11	
16	
21	
10	
80	
48	
39	
11	
3	
80	

## (15 pts) Exercise 7-17

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- Assume you have an empty cache with a total of 16 blocks, with each block having 2 bytes. In this exercise, the cache is two-way set associative. Assume LRU replacement.
- At right is a series of byte addresses. You should:
  1. Label each one as a hit or miss
  2. Draw the cache and show the final contents of the cacheAs always, show your work.

Address	Hit / Miss?
2	
3	
11	
16	
21	
10	
80	
48	
39	
11	
3	
80	